The EL4089 is a complete monolithic video amplifier sub-system in a single 8-pin package. It comprises a high quality video amplifier and a nulling, sample-and-hold amplifier specifically designed to stabilize video performance. The part is a derivative of Intersil's high performance video DC restoration amplifier, the EL2090, but has been optimized for lower system cost by reducing the pin count and the number of external components. For R_{GB} and YUV applications the EL4390 provides three channel in a single 16-pin package.

This application note provides background information on DC restoration. Typical applications circuits and design hints are given to assist in the development of cost effective systems based on the EL4089 and EL4390.

Video Signal Refresher

Composite Video Signal

Figure 2 represents a typical composite video signal, which has a standard distribution level of $1V_{P-P}$ into a 75Ω load, and comprises several sections. The video signal is the part containing the visible picture information, with a maximum

amplitude between black and white of 0.7V. At the end of the picture information is the front-porch, followed by a sync pulse, which is regenerated to provide system synchronization. The back-porch is the part of the signal that represents the black or blanking level. In NTSC color systems, the chroma or color burst signal is added to the back-porch and normally occupies 9 cycles of the 3.58MHz subcarrier.

DC Restoration—The Classical Approach

Video signals are often AC coupled to avoid DC bias interaction between different systems. The blanking level of the composite video signal therefore needs to be restored to an externally defined DC voltage, which locks the video signal to a predetermined common reference level, ensuring consistency in the displayed picture. This DC reference voltage, VR, sets and controls the picture brightness. The fundamental objective of the DC restore system is to force the DC output from the video amplifier to be equal to an externally defined reference voltage VR. Figure 3 shows a classical approach to DC restoration in video systems.
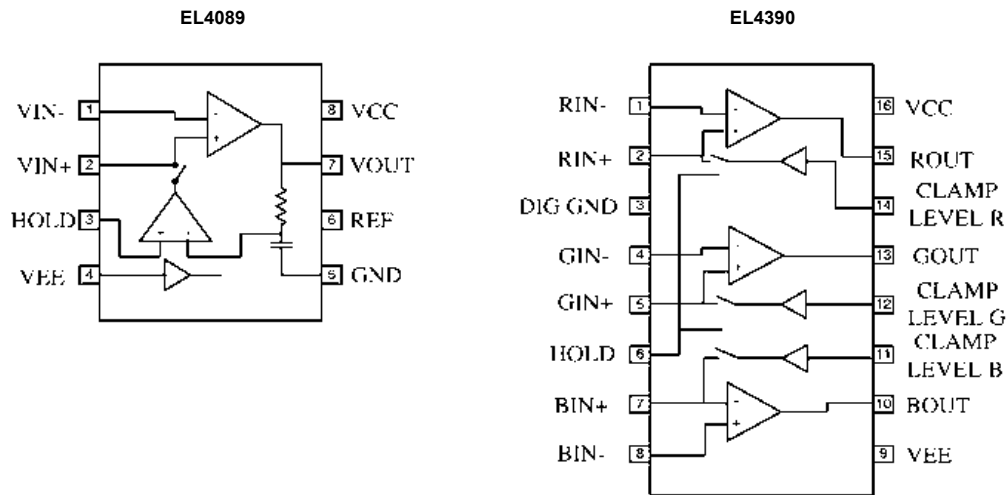
EL4089   **EL4390**

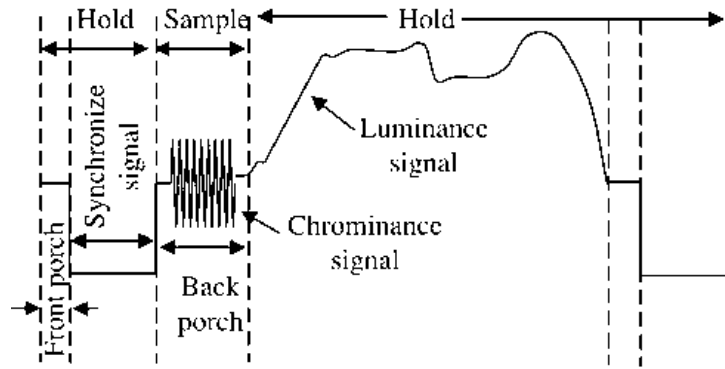**FIGURE 1. EL4089 AND EL4093 PACKAGE OUTLINES**
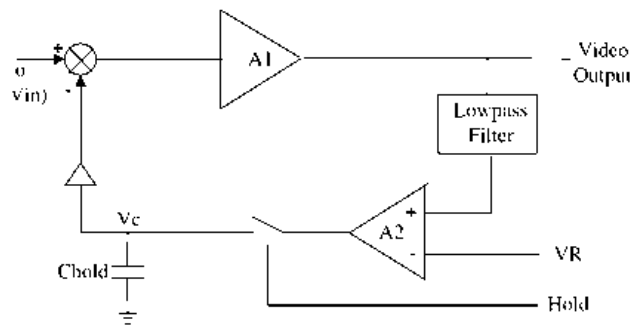
FIGURE 2. TYPICAL COMPOSITE VIDEO SIGNAL

FIGURE 3. CLASSICAL DC RESTORATION CONTROL SERVO LOOP

The Sync pulse is used to drive the control switch to the sample-and-hold, so that the DC servo loop is closed during the back-porch of the video signal. The lowpass filter is used to remove the chroma burst. The operation of the DC loop is perhaps best understood by considering the voltage appearing across the hold capacitor, C_{HOLD}. During the back-porch sampling period, the switch is closed and the hold capacitor charges up. It can be shown from the loop dynamics that

$$V_C = V_{IN} - \frac{VR}{A1} \qquad (EQ. 1)$$

where V_{IN} = VBP (the average back-porch voltage of the incoming video signal). Equation (1) can be reconfigured,

$$V_C = VBP - \frac{VR}{A1}$$

The net result is that

$$V_{OUT} \approx VR + \frac{VBP}{A2} \qquad (EQ. 2)$$

which shows that the output is clamped to VR with an offset term of VBP/A2. This offset is clearly small for a high gain DC loop amplifier, A2. During the hold period, the switch is open and the stored DC value of V_C is now subtracted from the incoming video signal, which effectively sets the back-

porch to VR and the video signal is amplified by the forward amplifier with gain, A1, giving

$$V_{OUT} = (V_{IN} - V_C)A1 = A1\left(V_{IN} - VBP + \frac{VR}{A1}\right)$$

$$V_{OUT} = A1(V_{IN} - VBP) + VR \qquad (EQ. 3)$$

DC Restoration—The EL4089 Approach

A simplified scheme of the EL4089 as a feedback system is shown in Figure 4. Unlike Figure 3, the input difference symbol is not shown because the error/correction voltage is stored across the coupling capacitor C_{HOLD} which is outside the control loop.

The operation of the EL4089 is simple, but very subtle. In sample mode, the amplifier's dynamics are such that the output is set to a predetermined reference voltage VR, which may be at ground potential. The correction voltage required at the input of amplifier A1 to maintain V_{OUT} at VR is simply stored across capacitor C_{HOLD}.
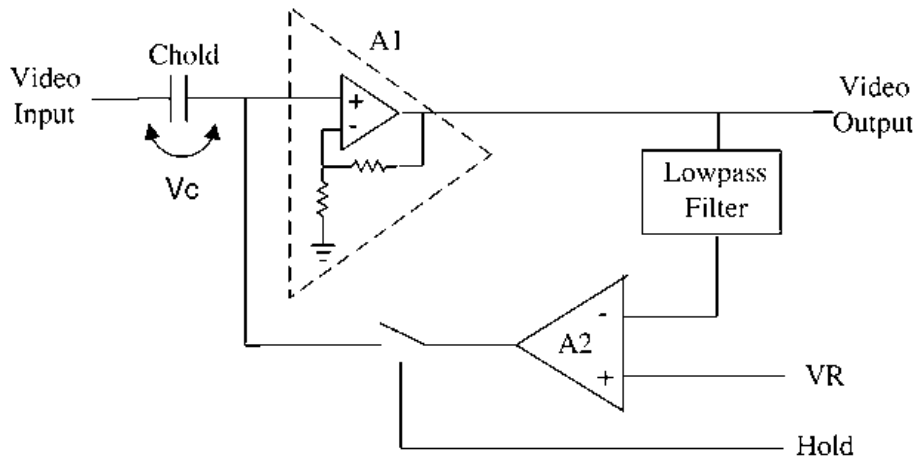
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FIGURE 4. SIMPLIFIED BLOCK DIAGRAM OF EL4089

Consider the following analysis. With the switch closed, the input voltage of amplifier A1 is (VR - V_{OUT})A2 giving V_{OUT} = (VR - V_{OUT})A1A2 and thus

$$V_{OUT} = VR\left\{\frac{A1A2}{1+A1A2}\right\} \approx VR \qquad \text{(EQ. 4)}$$

Assuming that the loop gain A1A2 is very high.

The correction voltage stored across capacitor C_{HOLD} is simply

$$VC = V_{IN} - (VR - V_{OUT})A2 \qquad \text{(EQ. 5)}$$

Assuming in this instance that V_{IN} = VBP, which is the average back-porch reference of the incoming signal, and substituting for V_{OUT} from Equations (4) and (5) gives

$$VC = VBP - \frac{VR}{A1} \qquad \text{(EQ. 6)}$$

Notice that the correction voltage VC is stored across that coupling capacitor C_{HOLD}, which is external to the loop amplifier. Unlike the classical system of Figure 3, it is this unique feature of the EL4089 which obviates the need for a classical sample-and-hold buffer amplifier in the feedback path; thus allowing a very economical 8-pin solution to be realized. Furthermore, the coupling capacitor has two functions, namely to avoid DC bias interaction between different systems and to hold the correction voltage as described above.

During the hold period, the video input signal (V_{IN}) is amplified in the classical way by the *2 video amplifier A1, but in this case the correction voltage held by C_{HOLD} is subtracted from the input to give

$$V_{OUT} = VR + (V_{IN} - VBP)A1 \qquad \text{(EQ. 7)}$$

Summary of Operation

1. When the HOLD logic input is set to TTL/CMOS logic 0, the sample-and-hold amplifier can be used to null the DC offset of the video amplifier.

2. When the HOLD input goes to a TTL/CMOS logic 1, the correcting voltage is stored on the video amplifiers input coupling capacitor. The correction voltage can be further corrected as need be, on each video line.

3. The video amplifier is optimized for video performance and low power. Its current-feedback design allows the user to maintain essentially the same bandwidth over a given gain range of nearly 10:1. The amplifier drives back-terminated 75Ω lines.

Subcircuits

The EL4089 DC restored amplifier is an 8-pin monolithic version of the circuit shown in Figure 4. The video amplifier, A1, is a 60MHz current feedback amplifier or CFA. These devices offer very high speed performance with excellent differential gain and phase. In many respects the CFA behaves as a conventional op-amp, but there are several key differences that must be considered by the user. In particular the two input impedances of the amplifier are different. The non-inverting input impedance is high and the inverting a low impedance. However, the special feature of the CFA is that when in a closed loop configuration, the feedback current is determined by the resistor, R_F, which controls that bandwidth of the amplifier independently of the gain setting resistor R_G.

The current feedback amplifier is essentially a transimpedance amplifier with an input voltage buffer to create a high input impedance non-inverting input. The transimpedance amplifier is formed by mirroring the output current of the input unity gain buffer into a high impedance internal Z-node and buffering this Z-node voltage through to a low impedance output, as shown schematically in Figure 5.
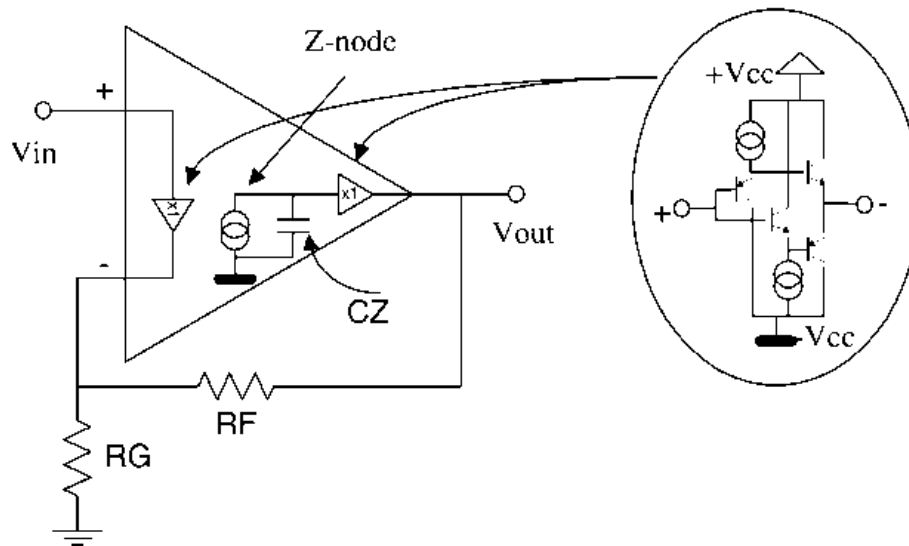
FIGURE 5. THE CURRENT-FEEDBACK OP-AMP

The unity gain buffers are a complementary class-AB common-collector stage, with DC current biasing. The slew-rate of the CFA is excellent due to the non-current limiting input stage. The CFA has only one internal high impedance node (Z), so it is essentially a single pole dominant amplifier. Since the inverting input terminal is the output terminal of a voltage buffer, it is a low impedance point and the feedback signal is current. Intuitively one can see that in closed loop the feedback current through R_F supplies the current demanded by R_G and the input error current into the inverting input terminal. It is this feedback current component of R_F which is used to charge the compensation capacitance at the Z-node. Theoretically it can be shown that the -3dB bandwidth is approximately,

$$f-3dB = \frac{1}{2pRFCZ}$$ (EQ. 8)

where CZ is the compensation capacitance of the Z-node. However, as for conventional op-amps, the closed loop gain, A1, is simply

$$A1 = 1 + \frac{R_F}{R_G}$$ (EQ. 9)

and the -3dB frequency can be controlled with R_F while the closed loop gain can be set independently with R_G.

The EL4390 Approach

The EL4390 is three high performance current feed-back amplifiers with DC restore function. A simplified schematic diagram of one of the channels in a DC restore configuration is shown in Figure 6. Its basic approach is very similar to the EL4089 in that the error/correction voltage is stored across the coupling capacitor C_{HOLD} from the video input to the positive input of the amplifier. Different from the EL4089, when the sample and hold switch is close, an internal buffer

amplifier is enabled to force the non-inverting input of the video amplifier to be equal to the reference input level. When the switch is open, an error voltage is stored on the input coupling capacitor C_{HOLD} to maintain the offset at the output. The following details the mathematical relationships between the inputs and output.

When the sample and hold switch is close,

$$V_{OUT} = A1 * VR$$ (EQ. 10)

where A1 is the close-loop gain of the amplifier.

The voltage across the hold capacitor is

$$VC = V_{IN} - VR$$ (EQ. 11)

In many NTSC video applications, the back-porch of the video signal is clamped. Thus, V_{IN} is the input back-porch level, VBP.

$$VC = VBP - VR$$ (EQ. 12)

When the sample and hold switch is open, the voltage across the hold capacitor maintains the proper offset.

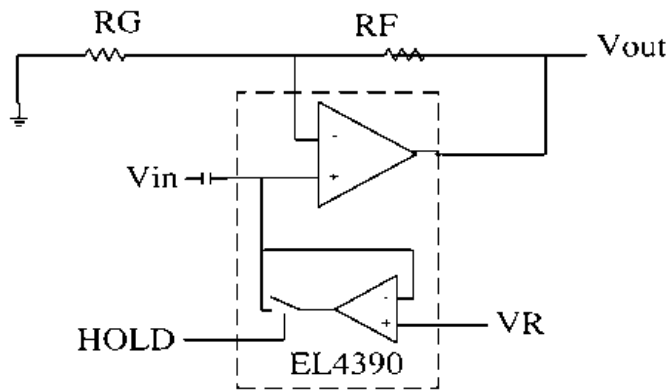$$V_{OUT} = A1(V_{IN} - VC) = A1 (V_{IN} - VBP + VR)$$ (EQ. 13)

FIGURE 6. SIMPLIFIED CONNECTION DIAGRAM OF EL4390

Features of the EL4089

Intersil pioneered the development of monolithic CFAs. As first to the market with the CFA our established reputation is confirmed with the EL4089 which is the first 8-pin monolithic DC restored video amplifier. A connection diagram for the EL4089 configured as a DC restoring amplifier with a gain of 2 restoring to ground (pin 3—zero voltage reference) is shown in Figure 7.

The EL4089 is fabricated in Intersil's proprietary Complementary Bipolar process which produces NPN and PNP transistors with equivalent AC and DC performance. The EL4089 is specified for operation over the 0°C to +75°C temperature range.

The on-chip current-feedback amplifier of EL4089 and EL4390 is optimized for video performance. Since it is a current-feedback amplifier, the -3dB bandwidth stays essentially constant for various closed-loop gains. The amplifier performs well at frequencies as high as 60MHz for the EL4089 and 80MHz for the EL4390 when driving 75Ω. The sample and hold circuit is optimized for fast sync pulse response.

Typical Application Circuits

The EL4089 and EL4390 are designed to DC-restore a video waveform (Figure 2). A typical application circuit of the EL4089 is illustrated in Figure 8. The following analysis also applies to the EL4390. This circuit forces the cable driving video amplifier's output to pin 3 reference voltage level when the HOLD pin is at a logic low. In the case of EL4390, when HOLD pin is logic low, the output of the video amplifier is driven to the reference voltage multiply by the close loop gain of the video amplifier. In Figure 8, pin 3 is grounded and HOLD pin is low during back-porch of the video signal, consequently, the back-porch is clamped to the ground voltage level.
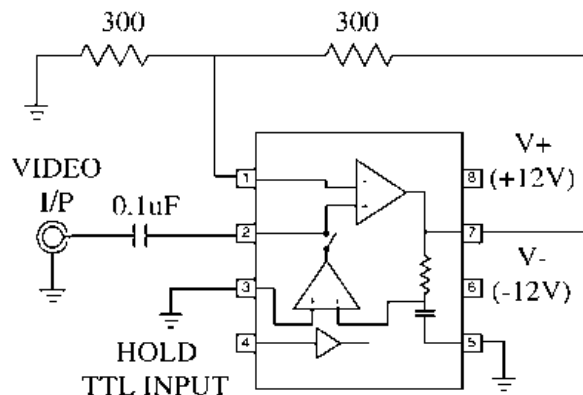

FIGURE 7. EL4089 CONNECTION DIAGRAM (CONFIGURED AS A DC RESTORING AMPLIFIER WITH A GAIN OF 2, RESTORING TO GROUND)
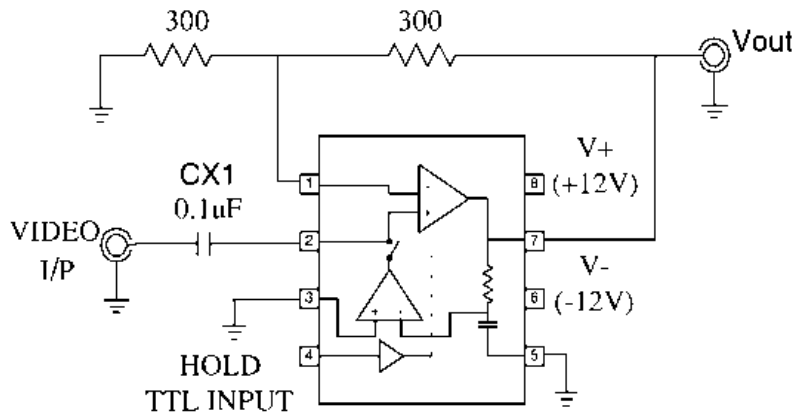
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FIGURE 8.

CX1 Determination

The correction voltage is stored across the capacitor CX1, an external ceramic capacitor connecting from the video signal input to the non-inverting input of the video amplifier. The following demonstrates how the CX1 capacitor should be chosen to satisfy the system droop voltage and sampling requirements.

Ideally the input impedance of the video amplifier should be infinite during the hold period to avoid any discharging effects on the CX1 capacitor. However, due to the inherent nature of the bipolar transistors, a bias current is always present. This bias current discharges CX1 during the hold time and as a result causes the correction voltage across CX1 to drift. Equation (14) gives the basic relationship between correction droop voltage and the CX1 value.

$$V(droop) = \frac{(I_B)(T_{LINE} - T_{SAMPLE})}{CX1} \qquad \text{(EQ. 14)}$$

Where:

   V(droop) is the voltage change across CX1 during hold period.

   I_B+ is the amplifier's non-inverting input bias current.

   T_{LINE} is the single video line duration.

   T_{SAMPLE} is the sampling time during which the S/H switch is closed.

The output voltage change due to voltage drooping is simply,

$V_{OUT}(droop) = V(droop) * A1$

Where:

   A1 is the close loop gain of the video amplifier.

In the Figure 8 design example, a typical input bias current of the video amplifier is 1μA, so for a 62μs hold time and 0.01μF capacitor, the correction voltage droops 6.2mV; consequently, the output voltage drifts by 12.4mV in one video line.

The CX1 value and sampling time also determine the amount of time required by the EL4089 to reach within its DC-restored voltage range.

$$V(ch\,arge) = I_{OUT}\frac{T_{SAMPLE}}{CX1} \qquad \text{(EQ. 15)}$$

Where:

   I_{OUT} is the sample and hold amplifier output current.

The sample and hold amplifier can typically provide a current of 300μA to charge CX1, so with 1.2μs sampling time, the output can be corrected by 36mV in each line.

Equations (14) and (15) demonstrate the trade-offs between CX1, sampling time, DC off-set droop voltage, and speed of the DC-restore function. Using a smaller value of CX1 increases both the voltages that can be corrected each line and the drift while being held, likewise, using a larger value of CX1 reduces those voltages.

In Figure 9, a resistor is connected from the non-inverting input of the amplifier to the negative supply to compensate for the non-inverting input bias current. To obtain the optimum performance, the compensation resistor R1 should be adjusted to give 0mV droop voltage at 50% field.

The restore current generated by the sample and hold amplifier decreases as the output voltage approaches the reference voltage. This effect combines with the 7mV of offset voltage error in the sample and hold amplifier can result in a 22mV of total error from the output to the reference voltage input during clamping. A method of correcting this problem is depicted in Figure 10. A voltage divider is used to compensate for the sample and hold amplifier offsets.

A complete DC-restore circuit with the EL4581 sync separator is shown in Figure 11. An optional RC low pass filter on HOLD input pin is included should the logic signal

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require slowing down. This RC network can also serve to prevent feet-through from the falling and rising edges of the back-porch sync timing signal to the video amplifier output. The video DC restore output and EL4581 back-porch timing waveforms are illustrated in Figure 12. During the back-

porch interval, the EL4581 pulls the hold pin of the EL4089 low and the EL4089 servo loop forces the output to the reference voltage level. In the photo, the input back-porch voltage level is 0.5V and the output back porch voltage level is restored to 0V, the reference voltage level.

Typical Application Circuits
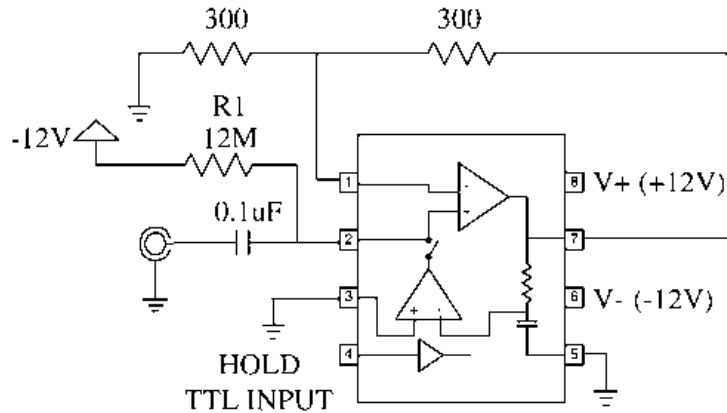
FIGURE 9. I_B+ BIAS CURRENT CORRECTION
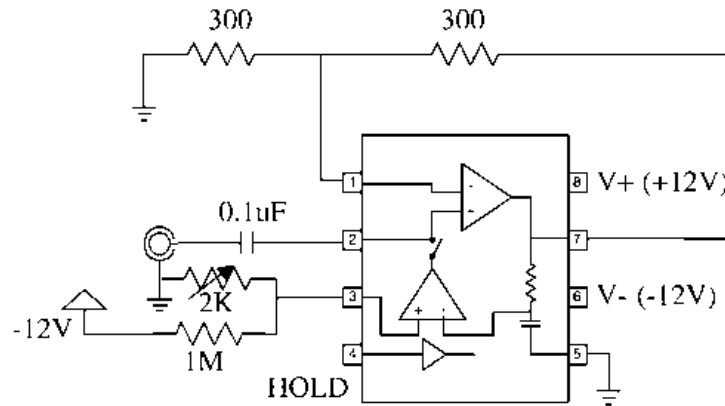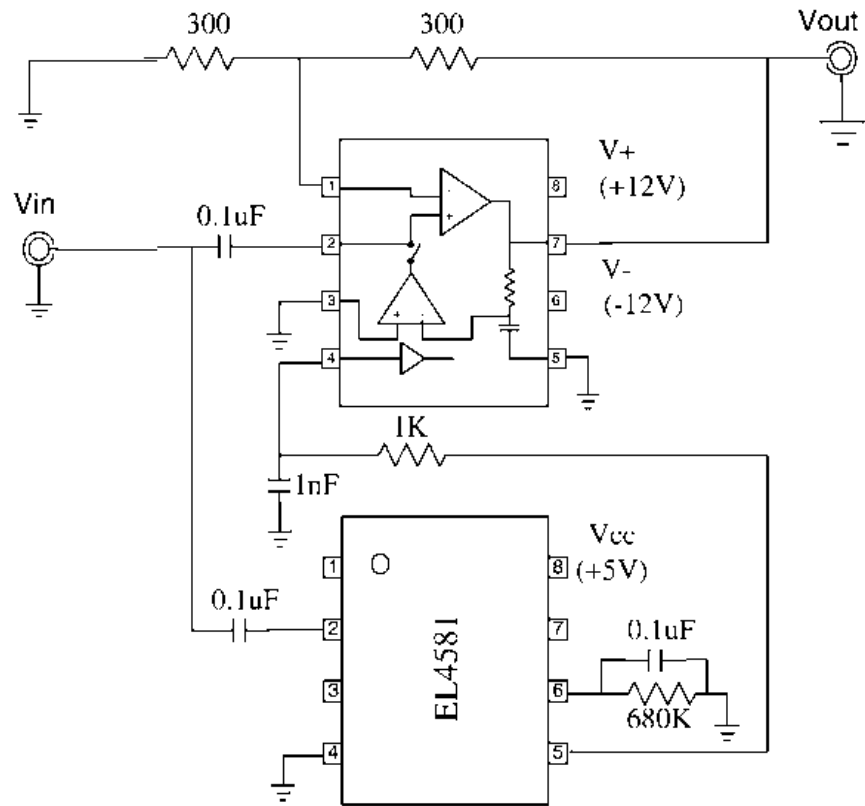

FIGURE 10. SAMPLE AND HOLD OFF-SET ERROR COMPENSATION

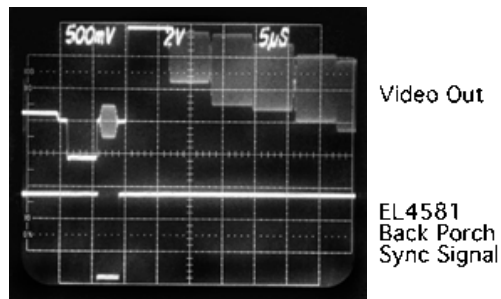**FIGURE 11. EL4581 AND EL4089 RESTORE AMPLIFIER AND SYNC SEPARATOR**

FIGURE 12. VIDEO OUTPUT AND EL4581 BACK-PORCH SYNC SIGNAL
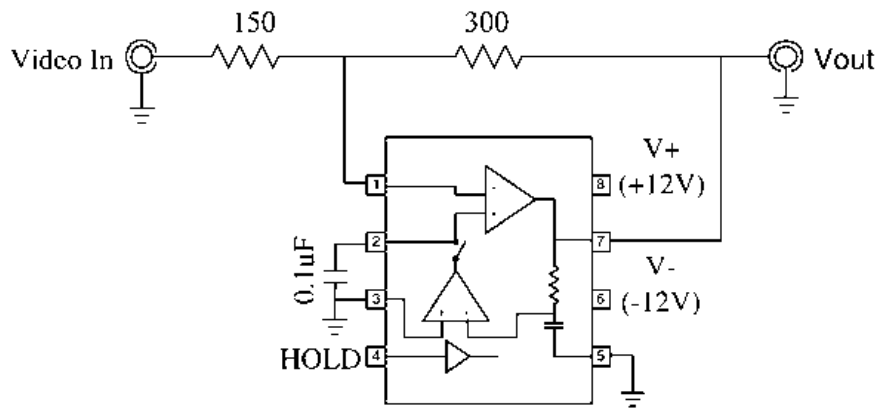
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FIGURE 13. EL4089 DC-RESTORE AMPLIFIER IN -2 GAIN CONFIGURATION

EL4089 in Inverting Gain Configuration

Placing the hold capacitor in the signal path leads to sync signal feed-through and phase distortion of the burst signal. Rearranging the EL4089 in the inverting configuration as shown in Figure 13 provides significant improvements. Figure 14 indicates a 15mV of voltage spike in amplifier output during the sampling interval and coincides with the falling and rising edge of the HOLD signal. The output voltage spike is caused by the charging current injecting out of the output of S/H amplifier during the back-porch interval. One way to minimize the sync feed-through is to feed the video input signal directly into the inverting input of the video amplifier and short the DC restore capacitor to ground. As a result, the video input signal is not affected by output current of the S/H amplifier. The voltage spike is also reduced by an addition of a simple RC network from the output of the EL4581 to the HOLD input of the EL4089. Figure 15 test result shows no voltage spikes and only a 4mV of voltage dip during the sampling period. In the inverting configuration, the video signal goes directly into a purely resistive component, thus, no phase shift occurs.
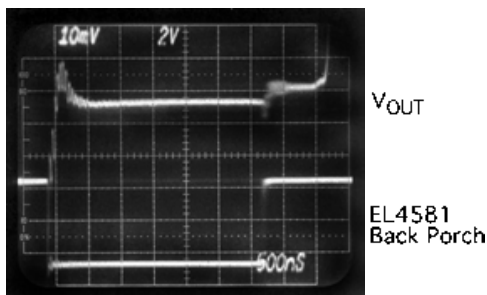

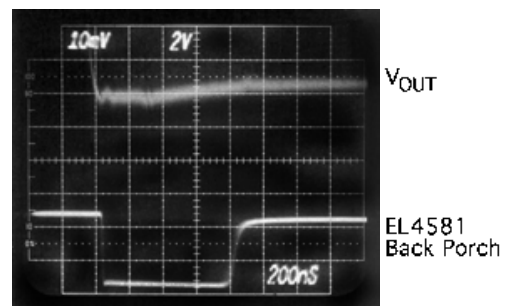
FIGURE 14. BACK-PORCH SYNC EDGE FEED-THROUGH

FIGURE 15. EL4089 INVERTING AMPLIFIER OUTPUT WAVEFORM

EL4581 Interface

The hold input of the EL4089 is designed to interface directly to Intersil's existing suite of sync separators, namely the EL4581 and the EL4583. The connection diagram of the EL4581 is shown in Figure 16.

The EL4581 extracts timing information including composite sync, vertical sync, burst/back-porch timing and odd/even field information from standard negative going sync NTSC, PAL, and SECAM video signals. The EL4581 detects video signals from 0.5 to 2V$_{P-P}$. The 50% slicing feature provides precise sync edge detection even in the presence of noise and variable signal amplitudes. A built-in linear phase, third order, color burst filter minimizes spurious timing information and reduces the number of external components. The integrated circuit is also capable of providing sync separation for non-standard, faster, horizontal rate video signals by changing an external horizontal scan rate setting resistor. The vertical output is produced on the rising edge of the first serration in the vertical sync period. A default output is produced after an internally generated time delay, in the event of missing serration pulses, for example, in the case of a non-standard video signal. All outputs are active low.

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Printed Circuit Board Layout Hints

The feedback path of the video amplifier should be kept as small as possible to avoid deterioration of high frequency gain accuracy.

The board layout should have a ground plane underneath the EL4089, with the ground plane cut away from the vicinity of the V_{IN}- pin (pin 1) to minimize the stray capacitance between pin 1 and ground.

Power supply bypassing is important and a 0.1µF ceramic capacitor, from each power pin to ground, placed very close

to the power pins, together with a 4.7µF tantalum bead capacitor, is recommended.

When both digital and analog grounds are on the same board, the EL4089 should be on the analog ground. The digital ground can be connected to the analog ground through a 100Ω–300Ω resistor near the EL4089. This allows the digital signal a return path while preventing the digital noise from corrupting the analog ground.
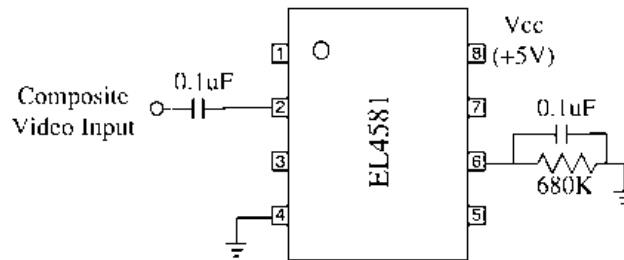

FIGURE 16. EL4581 CONNECTION DIAGRAM

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